AbstractID: 3357 Title: Theoretical and Empirical Investigations of Flat-Panel Imagers Incorporating Single- and Dual-Stage Pixel-Amplifiers Based on Polycrystalline Silicon Thin Film TFTs

Purpose: To investigate the potential for achieving significant improvements in DQE at low fluoroscopic exposures and high spatial frequencies, as well as at substantially higher frame rates, through the incorporation of novel pixel architectures based on polycrystalline silicon thin-film transistors (poly-Si TFTs).

Methods and Materials: Detailed studies were performed on the signal and noise characteristics of a series of arrays incorporating poly-Si TFTs. These indirect detection designs involved three pixel architectures with a standard circuit, with a single-stage amplifier, and with a dual-stage amplifier – along with a continuous photodiode structure. Determinations of MTF, NPS, and DQE, as well as of individual pixel properties (sensitivity, linearity, trapping, noise) were performed under fluoroscopic and radiographic conditions. Detailed studies of these and other hypothetical array designs were also performed using circuit simulation tools.

Results: These studies indicate that the high mobilities of poly-Si lead to potential frame rates at least an order of magnitude greater than those of conventional arrays with a-Si:H TFTs. In addition, the single-stage and dual-stage pixel-amplifier arrays exhibit signal gain (~×11 and ~×25, respectively) very close to that expected for these designs. Furthermore, while a net increase in the signal-to-noise performance was beyond the objective of these initial designs, analysis of the empirical data along with theoretical modeling strongly suggests that there are no intrinsic reasons precluding such performance enhancements. Finally, the non-destructive nature of the readout for pixel-amplifier designs enables repeated-signal-sampling, thereby creating new possibilities for noise reduction.

Conclusion: These results encourage the hypothesis that substantial improvements in DQE performance and readout speed are possible through the incorporation of poly-Si circuits into flat-panel pixel designs. Factors limiting the performance of present designs will be described and future steps in the development of this technology will be discussed. This work is supported by NIH grant R01 EB000558.